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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Application Number: 10/519,394

Filing Date: December 22, 2004

Appellant(s): SIEGELIN ET AL.

Pehr Jansson

For Appellant

EXAMINER'S ANSWER (Supplemental)

This is in response to the appeal brief filed 9/13/2010 appealing from the Office action mailed 3/16/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-10, 14-22, 32-33

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

WO 94/20906	Ban	9-1994
WO 95/10083	Assar et al.	4-1995
WO 01/88926	Mennecart	11-2001
WO 99/35650	Hazen et al.	7-1999
US 5758148	Lipovski	5-1998
US 4763305	Kuo	8-1988

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-2, 32-33,** rejected under 35 U.S.C. 102(b) as being anticipated by **Ban (WO 94/20906 hereinafter "Ban")**.

Consider **claim 1**, Ban discloses a method and computer readable storage medium to write in flash type memory *(flash memory, abstract; method (i.e., software, or firmware of hardware)…, page 2, lines 7-10)* of an electronic module comprising:

defining a mirror area in the flash type memory *(block, areas, units, or zones: page 2, line 21-page 3, line 15, page 3, lines 1-2)* divided into at least two physical areas *(flash memory physical address locations, page 2, line 21)* each designated to correspond to a same logical area for storing content written to the logical area *(fixed-length group of physical byte addresses form a logical block, page 3, lines 1-2; one or more physically contiguous flash memory areas or zones comprise a number of blocks, page 3, lines 4-7; therefore the physical byte addresses are associated with logical blocks, zones and units, FIG. 2, 3, & 7; Furthermore, there are a plurality of unique Logical areas associated with a fixed-length group of physical byte addresses: FIG. 3, 4, 7 and page 2, line 21-page 3, line 15)*;

designating one of the at least two physical areas as being an active physical area; and during a write *(abstract)* to said logical area, programming the content of said logical area into the active area *(flash*

memory system which "allows data to be continuously written to unwritten physical address locations," abstract; data cannot be written to an area of flash memory in which data has previously been written, unless the area is first erased, so the area is blank when programming page 1, lines 26-29) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).

Consider **claim 2**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium further comprising erasing the content of all physical areas in a memory area in a single operation at a convenient time *("One or more physically contiguous flash memory areas (called zones) that can be physically erased using suitable prior art flash memory technology comprise a unit and each unit contains an integral number of blocks," page 3, lines 4-7; there is a zone erase operation that erases the unit that includes that block, and unit containing the logical block consisting of multiple physical address locations are therefore all erased, the page 3, lines 24-25) (page 7, lines 1 - page 9, line 22 and page 13, claim 1).*

Consider **claim 32**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium wherein each physical area has a status which is one of three statuses *(each block denotes its status: page 7, lines 11-14; each block maps to physical address, therefore each physical area*

has a status: FIG. 4): blank *(block free and writable: page 7, line 13)*, active *(block allocates and contains user data: page 7, line 13-14)* and used *(block deleted and not writable: page 7, line 13)*.

Consider **claim 33**, and as applied to **claim 32** above, Ban discloses the method and computer readable storage medium wherein:

the blank status corresponds to one of the physical areas ready to receive data but not selected for receiving data *(block free and writable: page 7, line 13)*,

the active status corresponds to one of the physical areas ready to receive data and selected for receiving data or to one of the physical areas containing the actual content of the logical area to be read *(block allocates and contains user data: page 7, line 13)*,

the used status corresponds to one of the physical areas containing an outdated data that shall not be read, said physical area waiting for an erasure *(block deleted and not writable: page 7, line 13)*.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 3, 7-8, 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claims 1-2** above, and further in view of **Assar et al. (WO 95/10083 hereinafter "Assar").**

Consider **claim 3**, and as applied to **claim 2** above, Ban discloses the method wherein there is a convenient time as described above in claim 2.

However, Ban does not disclose the method comprising performing the erasure during a period of inactivity or when all the physical areas are used.

Assar discloses a method comprising performing an erasure when all the physical areas are used *(when physical memory is filled, blocks with certain flags set are erased, wherein as described above blocks contain multiple physical mirror areas, page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform an erasure when all the physical areas are used in the system of Ban, because Assar teaches it is necessary to erase some data when a memory is full in order to place new data in a flash memory *(page 20, lines 10-19)*.

Consider **claim 7**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium comprising designating said active physical areas *(active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1)*.

However, Ban does not disclose the method and computer readable storage medium comprising designating said active physical areas using a counter and incrementing the counter on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter *(counter 620 page 18, lines26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112)* and incrementing the counter on each change of active area *(page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a counter in the system of Ban, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next *(page 18, lines 26-28; abstract)*.

Consider **claim 8**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium of claim 1.

However, Ban does not disclose the method comprising associating at least one bit with a logical area to represent the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* to represent the use state of at least one physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area to represent the use state of at least one physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

Consider **claim 18**, and as applied to **claim 7** above, Ban in view of Assar discloses the method of claim 7.

However, Ban does not disclose the method comprising associating at least one bit with a logical area representing the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* representing the use state of at least one physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area representing the use state of at least one physical area of said logical area in the system of Ban, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

6. **Claim 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claim 1** above, and further in view of **Mennecart (WO 01/88926 A1 hereinafter "Mennecart").**

Consider **claim 4**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium of claim 1.

However Ban does not disclose the method comprising copying the active physical area into a buffer area, erasing all physical areas and copying the buffer into a first available physical area in the mirror area.

Mennecart discloses method comprising copying the active physical area into a buffer area *(buffer, abstract; step F5, temporary storage, FIG. 4)*, erasing all physical areas *(steps F3 and F3', FIG. 4)* and copying the buffer into a first available physical area *(page 5, line 1 – page 6, line 22; step F7, FIG. 4)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to copy the active physical area into a buffer area, erase all physical areas and copy the buffer into a first area available in the system of Ban, because Mennecart teaches the method to process a write command in memory such as EEPROM, a type of flash memory in smart cards, which reduces the time required for processing *(page 3, lines 9-35; abstract)*.

7. **Claim 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to claim **claim 2** above, and further in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen").**

Consider **claim 5**, and as applied to **claim 2** above, Ban discloses the method and computer readable storage medium comprising performing an erasure as described in claim 2.

However, Ban does not disclose the method comprising the erasure and programming/read operations in parallel thereby not blocking the electronic module.

Hazen discloses a method comprising programming/read operations in parallel thereby not blocking an electronic module *("read-while-write operations," title; abstract; page 2, paragraph 4; pages 5-7)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel with erasure thereby blocking an electronic module in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in terms of time constraints *(page 2, paragraph 2 and page 3, paragraph 1)*.

8. **Claim 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claim 5** above, and in view of **Lipovski (US Patent # 5758148)**.

Consider **claim 6**, and as applied to **claim 5** above, Ban in view of Hazen discloses the method and computer readable storage medium wherein comprises performing the erasure and programming/read operations in parallel, having mirror memory area(s), one area being used for programming/reading while the other area is erased as described above in claims 5 and 26.

However, Ban does not disclose the method and computer readable storage medium wherein comprises performing the erasure and programming/read operations in parallel **in a bi-bank memory**, said bi-bank memory corresponding to the mirror memory area each bank having mirror area(s), one bank being used for programming/reading while the other bank is erased, **changing active bank when all physical areas of the bank used for programming/read have been used.**

Hazen discloses the method wherein comprises performing the erasure and programming/read operations in parallel *(one device may be written to, while the other device is being erased, page 2, paragraph 3)* in a bi-bank memory *(multiple flash memory devices, page 2, paragraph 3)*, said bi-bank memory corresponding to the mirror memory area *(Ban teaches mirror memory areas in memory, while Hazen teaches bi-bank memory as a type of memory)* each bank

having physical area(s) *(as described in claims 5 and 26)*, one bank being used for programming/reading while the other bank is erased *(one device may be written to, while the other device is being erased, page 2, paragraph 3)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel in a bi-bank memory in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in term of time constraints *(page 2, paragraph 2; and page 3, paragraph 1)*.

Lipovski discloses a method of changing an active bank when all physical areas of the bank used for programming/read have been used *(one memory bank reaches its capacity, the system switches to the other bank to permit data writes, column 11, lines 38-42)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to change the active bank when all areas of the active bank have been used for programming operations in the system of Ban, because Lipovski teaches this allows to continue writing to memory without erasing the full memory bank *(column 11, lines 38-42)*.

9. **Claims 9-10** rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** as applied to **claims 1-2** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo").**

Consider **claim 9**, and as applied to **claim 1** above, Ban discloses the method and computer readable storage medium wherein the write is carried out as claim 1 above.

However, Ban does not disclose the method and computer readable storage medium, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area in the mirror area otherwise.

Kuo discloses a method, wherein if the content of the logical area is identical to the content of the active physical area, a write is carried out in an active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank

physical area otherwise, in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Consider **claim 10**, and as applied to **claim 9** above, Ban discloses the method and computer readable storage medium comprising programming *(writing)* of the logical area in the blank physical area in claim 1.

However, Ban does not disclose the method and computer readable storage medium comprising programming only a portion of the logical area in the blank physical area.

Kuo discloses a method comprising programming only part of the logical area in the blank physical area *(only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only part of the logical area in the blank physical area in the system of Ban, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

10. **Claims 14-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650**

hereinafter "Hazen") as applied to **claims 5 and 6** above, and further in view of **Assar et al. (WO 95/10083 hereinafter "Assar")**.

Consider **claims 14 and 15**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method comprising designating said active physical areas *(active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1)*.

However, Ban in view of Hazen does not disclose the method comprising designating said active physical areas using a counter and incrementing the counter on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter *(counter 620 page 18, lines26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112* and incrementing the counter on each change of active area *(page 20, lines 10-19)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a counter in the system of Ban in view of Hazen, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next *(page 18, lines 26-28; abstract)*.

Consider **claims 16 and 17**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses the method of claims 5 and 6.

However, Ban in view of Hazen does not disclose the method comprising associating at least one bit with a logical area to represent the use state of at least one physical area of said logical area.

Assar discloses a method comprising associating at least one bit *(one bit used flag 626, page 18, line 36)* with a logical area *(data block, page 18, lines 31-37)* to represent the use state of at least one physical area of said logical area *(page 18, lines 35-37)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate at least one bit with a logical area to represent the use state of at least one physical area of said logical area in the system of Ban in view of Hazen, because Assar teaches used/free flag is used to avoid an erase-before-write cycle and therefore avoid the overhead of an erase cycle *(page 7, lines 9-21)*.

11. **Claims 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Hazen et al. (WO 99/35650 hereinafter "Hazen")** as applied to **claims 5 and 6** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo")**.

Consider **claims 19 and 20**, and as applied to **claims 5 and 6** above, Ban in view of Hazen discloses wherein the write is carried out as claims 5 and 6 above.

However, Ban in view of Hazen does not disclose the method, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

12. **Claim 21-22** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ban (WO 94/20906 hereinafter "Ban")** in view of **Assar et al. (WO 95/10083 hereinafter "Assar")** as applied to **claim 7** above, and further in view of **Kuo (US Patent # 4763305 hereinafter "Kuo").**

Consider **claim 21**, and as applied to **claim 7** above, Ban in view of Assar discloses wherein the write is carried out as claim 7 above.

However, Ban in view of Assar does not disclose the method, wherein if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area, and in a blank physical area otherwise.

Kuo discloses a method, wherein a write is carried out in an active physical area if the content of the logical area is identical to the content of the active physical area *(if data in the area is the same as the data to be written, then avoid the erase/program cycle the data and the write is complete for that area, column 6, lines 18-26)*, and in a blank physical area otherwise *(if old data in byte or block is already in erased state or blank, or the data does not match so the physical area is erased or blank and then the write is performed; column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include when the write is carried out in an active physical area if the content of the logical area is identical to the content

of the active physical area or when said write involves no erasure, and in a blank physical area otherwise, in the system of Ban in view of Assar, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

Consider **claim 22**, and as applied to **claim 21** above, Ban in view of Hazen and Kuo discloses the method comprising programming *(writing)* of the logical area in the blank physical area in claim 1.

However, Ban in view of Hazen does not disclose the method comprising programming only a portion of the logical area in the blank physical area.

Kuo discloses a method comprising programming only a portion of the logical area in the blank physical area *(only erase/program those areas which need to be, those areas that new data is same as old do not need to be erased and subsequently reprogrammed, column 5, lines 62-68 and column 6, lines 18-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to be able to program only a portion of the logical area in the blank physical area in the system of Ban in view of Hazen, because Kuo teaches this saves the time normally required to perform the erase *(column 6, lines 29-30)*.

(10) Response to Argument

Appellant describes the prior art and current application's Specification in pages 5-16.

Claim 1: Appellant argues against prior art teaching claimed: "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area"

Appellant argues against the prior art teaching "defining a mirror area". However it appears Appellant is reading much into the claims and argues the term "mirror area" as if it means something other than as claimed. Appellant's specification recites something similar to the claim language: "This invention concerns a method to write in a Flash type memory of an electronic module characterised in that it consists in associating at least two physical areas of said memory, called mirror areas, with the same logical area and during a write in said logical area" *(Current application specification: page 2, summary of the invention)* and "associating at least two physical areas of said memory, called mirror areas, with the same logical area and during a write in said logical area, in programming the content of said logical area in one of said blank mirror areas" *(current application specification: abstract)*. This is what the specification describes a mirror area as. There is no defining of the term besides these excerpts and the limitations in the claims.

Claim 1 merely recites: "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area". As such applicant is defining the term,

mirror area, as being divided into at least two physical areas corresponding to a same logical area for storing data. A logical definition or mapping of one logical area (zone, block, unit, etc.) to at least two physical areas (addresses, blocks, etc...) clearly reads on the claim language.

Ban discloses physical areas (physical byte addresses) each designated to correspond to a same logical area (zone and/or logical block) for storing content written to the logical area *(page 3, lines 1-7)*. Applicant appears to reading into the claim language *(appeal brief: page 16, lines 13-16)* that Ban's "logical block" must correspond to Applicant's area *(although it is not clear on which of the plurality of areas being argued and claimed)*. However, the claim language does not recite or require this mapping.

Appellant's arguments on page 16, lines 8-16 of the appeal brief are unclear. It appears that Appellant assumes "defining a mirror area" contains some extra meaning such as the "defining" is actually predefining a physical area upon fabrication of the memory or some sort. However, this is clearly not required by the current claim language nor is the mirror area required to be interpreted as such in view of the specification. The claim merely recites: "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area". While Ban teaches defining areas by mapping physical addresses to blocks, zones and units *(Ban: FIG. 2, 3, 4, 7 and page 2, line 21-page 3, line 15)*.

The term used "mirror area" is not the common use of the term. A mirror area to one of ordinary skill would normally be an area of memory containing copies or duplicates of the exact same data. For instance RAID 1 is a type of mirroring wherein every memory area of the primary memory is mirrored to a secondary memory thereby containing exact copies of the data for the purposes of redundancy. Appellant's arguments and Specification (ie. FIG. 3) clearly merely describe a *mirror area* as a generic area defined to be divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area. The term "mirror area" holds no patentable weight, but the claim language defining the term does: "divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area ".

Claim 1: Appellant argues against prior art teaching claimed: "designating one of the at least two physical areas as being an active area"

Appellant argues on page 16, line 17 through page 17, line 2 for the same reasons as before *(interpretation of "defining a mirror area")* as described above. Examiner respectfully disagrees. See above response. A logical unit, zone, or block corresponds to multiple physical byte addresses as described above. Also a mirror area is not defined to be a physical area predefined upon fabrication of the memory as it appears the Appellant intends. Once the mapping and programming of the logical area to physical byte addresses occurs, all and therefore one of the at least two physical byte addresses are designated as being an active area *(Ban: page 3, lines 1-7, pages 7-9;*

FIGS. 3-4, 6). The claim language does not limit the interpretation to *only one* of the at least two physical areas being designated as the active area

Claim 1: Appellant argues against prior art teaching claimed: "during a write to said logical area, programming the content of said logical area into the active physical area"

Appellant argues on page 17, line 3 through page 17, line 9 for the same reasons as above *(That Ban does not teach defining a mirror area)*. Examiner respectfully disagrees. See above response. A logical unit or block corresponds to multiple physical byte addresses as described above. And the claim limitations do not claim "only" one of the at least two physical areas as being an active physical area, as it appears Applicant is arguing. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim 1: Appellants arguments continued, page 17-18 of appeal brief

Appellant argue "Appellants claim defining, in a physical space, areas that are mirror areas that are divided into physical areas that each correspond to the same logical area for storing the same content written to the logical area." In response to applicant's argument that the references fail to show certain features of applicant's

invention, it is noted that the features upon which applicant relies (i.e., “defining, in a physical space, areas that are mirror areas”…) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim language is interpreted as described above and Examiner asserts Ban teaches the claim language as shown above.

Appellant argues Ban teaches an addressing hierarchy which is "never meant to store the same content as one particular logical area but rather to store portions of a logical area” *(appeal brief page 17, line 20 through page 18, line 2)*. However, this is irrelevant since the claim language does not reflect such argument. In Ban, a logical unit, zone, or block corresponds to multiple physical byte addresses as described above. Also a mirror area is not defined to be a physical area predefined upon fabrication of the memory as it appears the Appellant intends. Once the mapping and programming of the logical area to physical byte addresses occurs, all and therefore one of the at least two physical byte addresses are designated as being an active area *(Ban: page 3, lines 1-7, pages 7-9; FIGS. 3-4, 6)*. The claim language does not limit the interpretation to *only one* of the at least two physical areas being designated as the active area.

Claims 2, 32, and 33

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

Ban in view of Assar

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Examiner relies on Ban and Assar to teach the claim limitations of claim 3 and not solely on Assar as Appellant argues. Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

Specifically Appellant is arguing that Assar fails to teach the defining a mirror area for the same reasons that Appellant asserts Ban fails to teach such. Examiner respectfully disagrees. See above response. Examiner relies on Assar to teach a method of memory operation comprising performing an erasure when all the physical areas are used *(when physical memory is filled, blocks with certain flags set are erased, wherein as described above blocks contain multiple physical mirror areas, page 20, lines 10-19)*. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform an erasure when all the physical areas are used in the system of Ban, because Assar teaches it is necessary to erase

some data when a memory is full in order to place new data in a flash memory *(page 20, lines 10-19)*.

Claim 3

Appellant argues for same reasons as described above in section "Ban in view of Assar" including the "defining a mirror area" limitation of claim 1. See above responses. Appellant argues:

> "Assar states that "periodically the memory storage will fill" thus implying that the entire memory storage is full and not merely a mirror area. Thus, Assar does not teach or suggest that any erase operations cannot be triggered by "when all the physical areas [of the mirror area] are used."

Examiner relies on Ban teach a mirror area as described above and Assar to teach performing an erasure when all the physical areas are used. If all the physical areas of the memory are full, then off course all the physical areas of the mirror are full or used.

Claim 7

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., description of FIG. 3 of current application and "the area is "divided" it may be inferred that the blocks are contiguous in the physical address space", "erasure is the very act that is avoided"; pages 20-22 of appeal brief) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim merely recites: designating said active physical area using a counter and incrementing the counter on each change of the active area. Appellant appears to be reading language into the claim which is not present.

Ban discloses the method and computer readable storage medium comprising designating said active physical areas *(active unit made up of active blocks, FIG. 7; page 9, lines 27-30; page 10, line 1)*. However, Ban does not disclose the method and computer readable storage medium comprising designating said active physical areas using a counter and incrementing the counter on each change of active area.

Assar discloses a method comprising designating active physical areas using a counter *(counter 620 page 18, lines26-page 19, line 1; page 20, line 17 and 26; counter 620 is used in conjunction with flags such as the used/free flag 112)* and incrementing the counter on each change of active area *(page 20, lines 10-19)*. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to designate active physical areas using a counter in the system of Ban, because Assar teaches a counter is used to show the number of times a block has been erased and written (which areas are most and least worn out) in order to determine where to write next *(page 18, lines 26-28; abstract).*

Ban in view of Mennecart

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

In response to applicant's arguments against the references individually *(page 23, lines 4-13 of appeal brief)*, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Examiner relies on Ban and Mennecart to teach the claim limitations of claim 4 and not solely on Assar as Appellant argues. Examiner relies on Ban to teach the limitations of claim 1 including defining a mirror area and relies on Mennecart to teach copying the active physical area into a buffer area *(buffer, abstract; step F5, temporary storage, FIG. 4)*, erasing all physical areas *(steps F3 and F3', FIG. 4)* and copying the buffer into a first available physical area *(page 5, line 1 – page 6, line 22; step F7, FIG. 4)*. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to copy the active physical area into a buffer area, erase all physical areas and copy the buffer into a first area available in the system of Ban, because Mennecart teaches the method to process a write command in memory such as EEPROM, a type of flash memory in smart cards, which reduces the time required for processing *(page 3, lines 9-35; abstract)*.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., "Mennecart does not teach allocating a new physical area for writing into" page 23) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Mennecart does teach allocating a new physical area for writing to, since the buffer is a new physical area.

Ban in view of Hazen

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

Ban in view of Hazen in view of Lipovski

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

In response to applicant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir.

1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). In this case, Ban may not disclose the method comprising the erasure and programming/read operations in parallel thereby not blocking the electronic module. Hazen discloses a method in the same field of endeavor of computer memory and storage comprising programming/read operations in parallel thereby not blocking an electronic module *("read-while-write operations," title; abstract; page 2, paragraph 4; pages 5-7).*Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use programming/read operations in parallel with erasure thereby blocking an electronic module in the system of Ban, because Hazen teaches simultaneous operations is desired and an advantage in a flash memory device in terms of time constraints *(page 2, paragraph 2 and page 3, paragraph 1).*

Both references pertain to computer memory operations. Furthermore, Flash RAM is a synonym for Flash memory. Hazen teaches simultaneous or parallel operations which decreases the time it would take if the operations are initiated sequentially *("read-while-write operations," title; abstract; page 2, paragraph 4; pages 5-7).*

Ban in view of Kuo

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

Other Combinations

Appellant argues the claims for the same reasons as claim 1. Examiner respectfully disagrees. See above detailed response which specifies why Ban teaches the limitations of claim 1.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Matthew R Chrzanowski/

Examiner, Art Unit 2186

Conferees:

/Manorama Padmanabhan/ QAS, TC2100, WG2180
/Matt Kim/ Supervisory Patent Examiner, Art Unit 2186